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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,296	10/08/2003	Hisaki Kurashina	110826.02	4228
25944	7590	03/18/2004	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			SCHECHTER, ANDREW M	
			ART UNIT	PAPER NUMBER
			2871	

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/680,296	KURASHINA, HISAKI	
	Examiner	Art Unit	
	Andrew Schechter	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 8 is/are rejected.
- 7) ☒ Claim(s) 3-7 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 10/005,147.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>20031008</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Electro-optical device having storage capacitor laminated between data line and pixel electrode".

Claim Objections

2. Claim 4 is objected to because of the following informalities: the phrase "a barrier layer forming a film of the data line" is unnecessarily confusing; it refers to, for instance, the barrier layer 705 [see p. 35, paragraph 0134 of the specification], and should read "a barrier layer formed of the same film as the data line" or similar.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by *Ohtani et al.*, U.S. Patent No. 6,313,481.

Ohtani discloses [see Figs. 11 and 12] an electro-optical device comprising, above a substrate [900]: scanning lines [903 “gate wiring”] and data lines [908 “source wiring”] that intersect with each other to form a grid-like pattern [see Fig. 5A, for instance, showing the gate and source wiring intersecting to form a grid, which is the case for each embodiment of *Ohtani* – col. 10, lines 36-38, col. 14, lines 11-15]; thin film transistors [col. 14, lines 31-32], each of the thin-film transistors disposed in correspondence with intersections of one of the scanning lines and one of the data lines [again, see Fig. 5A]; pixel electrodes [923] respectively being disposed in correspondence with the thin film transistors [see Fig. 12C]; a first light shielding film [917] laminated between the data line and the pixel electrode; and a storage capacitor [917 and 911, see Fig. 12C, col. 15, lines 19-38] including the first light shielding film, laminated between the data line and the pixel electrode. Claim 1 is therefore anticipated.

Ohtani discloses an electronic apparatus comprising this device, so claim 8 is also anticipated.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Ohtani et al.*, U.S. Patent No. 6,313,481 as applied to claim 1 above, in view of *Nakamura et al.*, U.S. Patent No. 5,986,723.

Ohtani does not explicitly disclose the additional limitation of claim 2, that the TFT has a channel region which is formed in an intersection portion of the scanning and data lines. *Ohtani* instead states that the "present invention does not depend on the 'TFT structure', which allows the TFT to be formed by every known method" [col. 6, lines 11-13]. *Nakamura* does disclose [see Figs. 1 and 2] a TFT having a channel region [130] which is formed in an intersection portion of the scanning line [17] and data line [14]. It would have been obvious to one of ordinary skill in the art at the time of the invention to form the TFT by the method of *Nakamura*, motivated by *Nakamura's* teaching that its TFT structure, with its channel region at the intersection of the scanning and data lines, and particularly underneath the data (signal) line, shields the channel region from incident light, thus avoiding leakage currents due to light irradiation which would degrade the display quality [col. 8, lines 7-12]. Claim 2 is therefore unpatentable.

Allowable Subject Matter

7. Claims 3-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

The prior art, in particular *Ohtani*, does not disclose the device of claim 3, in particular the additional limitation that the storage capacitor comprises the first light shielding film and a capacitive electrode of pixel-electrode potential. (In *Ohtani*, the first light shielding film is of pixel-electrode potential, not the capacitive electrode.) Claim 3 would therefore be allowable if rewritten appropriately, as would claims 4 and 5 which depend from it.

The prior art, in particular *Ohtani*, does not disclose the device of claim 6, in particular the additional limitation that the first light shielding film is formed along the scanning line and the data line. (The examiner notes that the first light shielding film of *Ohtani*, as shown in Fig. 12C connected to the pixel electrode, cannot be extended in a grid form to cover the whole array, else it would short out the different pixel electrodes; and as shown in Fig. 12D not connected to the pixel electrode, it could be extended in a grid form, but it does not constitute a "storage capacitor including the first light shielding film" as required by claim 1.) Claim 6 would therefore be allowable if rewritten appropriately, as would claim 7 which depends on it.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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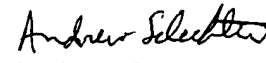
U.S. Patent No. 6,327,006 to *Sato et al.* discloses [see Fig. 3] an LCD with first light shielding film [4M] laminated between the data line and the pixel electrode, forming a storage capacitor with the data line below it. Since the storage capacitor includes the data line, it is not laminated between the data line and the pixel electrode as recited by claim 1.

U.S. Patent No. 6,271,543 to *Ohtani et al.* discloses [see Fig. 12] an LCD with first light shielding film [1206] laminated between the data line and the pixel electrode, forming a storage capacitor with the pixel electrode above it. Since the storage capacitor includes the pixel electrode, it is not laminated between the data line and the pixel electrode as recited by claim 1.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Andrew Schechter
Patent Examiner
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17 February 2004